Claims:

1. A random number generator, comprising an electrical circuit that has an unstable state and a stable state which it settles into after a random period of time; a counter that determines the time that it takes for the electrical circuit to settle into the stable state; and a generator that generates a random number using the settle time as the random seed.

2. The generator of Claim 1, wherein the electrical circuit starts in the unstable state when power is applied to the electrical circuit.

3. The generator of Claim 1, wherein the electrical circuit is forced into the unstable state during the operation of the electrical circuit in order to generate a new random seed.

4. The generator of Claim 2, wherein the electrical circuit comprises a phase locked loop.

5. The generator of Claim 4, wherein the counter further comprises a counter that counts the number of meta-stable clock ticks of the phase locked loop during the settle time of the phase locked loop and wherein the random seed comprises the number of meta-stable clock ticks of the phase locked loop during the settle time.

6. A random number generation method, comprising:

providing an electrical circuit that has an unstable state and a stable state which it settles into after a random period of time;

counting the time that it takes for the electrical circuit to settle into the stable state; and

generating a random seed based on the settle time of the electrical circuit.

7. The method of Claim 6 further comprising applying power to the electrical circuit so that the electrical circuit starts in the unstable state when power is applied to the electrical circuit.

8. The method of Claim 6 further comprising causing the electrical circuit to be placed into the unstable state during the operation of the electrical circuit in order to generate a new random seed.

9. A random seed generator, comprising:

an electrical circuit that has an unstable state and a stable state which it settles into after a random period of time; and

a counter that determines the time that it takes for the electrical circuit to settle into the stable state wherein the settle time corresponds to a random seed for generating a random number.

10. The generator of Claim 9, wherein the electrical circuit starts in the unstable state when power is applied to the electrical circuit.

11. The generator of Claim 9, wherein the electrical circuit is forced into the unstable state during the operation of the electrical circuit in order to generate a new random seed.

12. The generator of Claim 10, wherein the electrical circuit comprises a phase locked loop.

13. The generator of Claim 12, wherein the counter further comprises a counter that counts the number of meta-stable clock ticks of the phase locked loop during the settle time of the phase locked loop and wherein the random seed comprises the number of meta-stable clock ticks of the phase locked loop during the settle time.

14. A random seed generation method, comprising:

providing an electrical circuit that has an unstable state and a stable state which it settles into after a random period of time; and

counting the random time that it takes for the electrical circuit to settle into the stable state wherein the settle time corresponds to a random seed for generating a random number.

15. The method of Claim 14 further comprising applying power to the electrical circuit to put the electrical circuit into the unstable state.

16. The method of Claim 14 further comprising causing the electrical circuit to enter the unstable state during the operation of the electrical circuit in order to generate a new random seed.

17. A computer system that generates a random number, comprising:

a phase locked loop circuit that has an unstable state and a stable state that it enters after some random period of time;

a counter for determining the period of time for the phase locked loop to settle into the stable state, the settle time corresponding to a random seed; and

a generator for applying the random seed to a random number generator in order to generate a random number.

18. The computer system of Claim 17, wherein the counter further comprises a counter that counts the number of meta-stable clock ticks of the phase locked loop during the settle time of the phase locked loop and wherein the random seed comprises the number of meta-stable clock ticks of the phase locked loop during the settle time.